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EXAMINER	
WILLIAMS, LAWRENCE B	
ART UNIT	**PAPER NUMBER**
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/692,040	NAGARAJA, SRIKANTH	
	Examiner	Art Unit	
	Lawrence B. Williams	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10,12-15,18-34, 36-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15, 18- 22* is/are allowed.

6)☒ Claim(s) *1,4,8-10,13,23,24,34,37 and 38* is/are rejected.

7)☒ Claim(s) *5-7,12,14,25-29,31-33,36,39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 23, 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Hadad (US Patent 6,985,432 B1).

(1) With regard to claim 23, Hadad discloses in Fig. 3, a clock correction module in a local receiver to synchronize a local receiver clock, in the local receiver, with a remote transmitter clock, in a remote transmitter, in a multi-carrier communication system, while transmitting a data signal by the remote transmitter, comprising: a data sampler (Fig. 3, Pilot Ext, 27) to sample an input pilot signal of a predetermined carrier frequency and phase (col. 8, lines 47-50); a frequency drift estimator (AFC; col. 6, lines 35-37), coupled to the data sampler, to receive the data signal along with the input pilot signal, and to estimate a frequency drift between the receiver and transmitter clocks using the input pilot signal; a phase drift estimator (ASC; col. 6, lines 15-24), coupled to the data sampler and the frequency drift estimator, to receive the data signal along with the input pilot signal, and to estimate a phase drift between the receiver and transmitter clocks using the input pilot signal; an analyzer, coupled to the frequency drift

estimator (AFC, col. 9, lines 61-65; Hadad discloses the AFC detects a frequency error from the pilots and issues a correction signal (clock correction parameter). Thus the AFC also acts as an analyzer since a frequency error is detected and based upon this frequency error, a corrected timing signal is created) and the phase drift estimator (Hadad discloses the ASC detects the slope of the phase of the pilots and computes a synchronization error, and supplies a corrected timing signal (clock correction parameter). Thus the ASC also functions as an analyzer, since it detects the slopes of the phase of the pilots and based upon this phase computes an error and supplies a corrected timing signal) to receive the estimated phase and frequency drifts, and to compute a clock correction parameter (both ASC and AFC compute a corrected timing signal) based on the received estimated phase and frequency drifts; and a synchronizing block (NCO, 26, VCO, 23), coupled to the analyzer, to receive the clock correction parameter, and to adjust the receiver clock to synchronize the receiver clock with the transmitter clock based the clock correction parameter (col. 9, lines 22-30, 56-65).

(2) With regard to claim 30, claim discloses limitations similar to those disclosed in claim 23. Therefore a similar rejection applies.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 10, 34, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hadad (US Patent 6,985,432 B1) in view of Kleider et al. (US Patent 6,487,252 B1).

(1) With regard to claim 1, Hadad discloses in Fig. 3, a method for synchronizing a receiver clock with a transmitter clock in a communication system, during transmission of a data signal by a transmitter, comprising: obtaining estimates of frequency (AFC; col. 6, lines 35-37) and phase drifts (ASC; col. 6, lines 15-24) between the transmitter and receiver clocks; and synchronizing the receiver clock (NCO, 26; VCO, 23) with the transmitter clock based on the estimated phase and frequency drifts (col. 6, lines 20-24, 44-46); wherein synchronizing the receiver and transmitter clocks comprises: receiving an input pilot signal (Pilot Ext., 27) of a predetermined frequency and phase (col. 8, lines 47-50), by a receiver (Fig. 3) from the transmitter; estimating the frequency (col. 6, lines 35-37) and phase drifts (col. 6, lines 20-24) between the transmitter and the receiver clocks using the input pilot signal (col. 9, lines 22-24); computing a clock correction parameter based on the phase and frequency drifts; and synchronizing the receiver clock with the transmitter clock based on the clock correction parameter (col. 9, lines 22-30; lines 56-66).

Hadad does not disclose estimating a window length using the input pilot signal; forming a window using the window length for sampling the input pilot signal for estimating the frequency and phase drifts; estimating the frequency and phase drifts between the transmitter and the receiver clocks using the window; computing the clock correction parameter

based on the phase and frequency drifts; synchronizing the receiver and transmitter clocks based on the clock correction parameter.

However, Kleider et al. discloses in Fig(s). 7A-7C, a method for synchronization wherein he discloses estimating a window length using the input pilot signal (Kleider et al. discloses choosing an appropriate window resolution for y(n) (col. 10, lines 30-32; Kleider et al. also discloses y(n) containing an input pilot sequence (col. 7, lines 65-66)); forming a window using the window length (Fig(s). 7A-7C) for sampling the input pilot signal for estimating the frequency and phase drifts; estimating the frequency and phase drifts between the transmitter and the receiver clocks using the window (col. 10, lines 30-33; Kleider et al. discloses timing (phase) and frequency offsets; also lines 43-53); computing the clock correction parameter based on the phase and frequency drifts; synchronizing the receiver and transmitter clocks based on the clock correction parameter (Fig. 6, col. 6, line 60-col. 7, line 8; Kleider et al. discloses clock recovery (synchronization of transmitter and receiver clocks) based on sampling instant offset estimates (phase drift) and frequency offsets).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Kleider et al. as a method of synchronization and correcting timing alignment for multicarrier signals (col. 1, lines 34-37).

(2) With regard to claim 4, Kleider et al. also discloses repeating the estimating, computing, and synchronizing steps for a next window (Fig. 7A-7C discloses example window lengths used for estimation of the offsets (pg. 10, lines 20-36). It would simply be inherent that the process would be repeated for each window.

(3) With regard to claim 10, Hadad discloses in Fig. 3, a method for synchronizing a

receiver clock with a remote transmitter in a multi-carrier transmission system, comprising: obtaining estimates of frequency (AFC; col. 6, lines 35-37) and phase drifts (ASC; col. 6, lines 15-24) between the transmitter and receiver clocks; and synchronizing the receiver clock (NCO, 26; VCO, 23) with the remote transmitter clock based on the estimated phase and frequency drifts (col. 9, lines 22-30; lines 56-66) during transmission of a data signal by the remote transmitter (col. 6, lines 15-19, 37-38; Hadad discloses the operation during real time which would include both transmission and reception times.

Hadad does not disclose wherein synchronizing the receiver and transmitter clocks comprises: obtaining a window length from an experimental knowledge base; forming a window using the window length; estimating the frequency and phase drifts between the transmitter and the receiver clocks using an input pilot signal and the window; computing a clock correction parameter based on the phase and frequency drift estimates; synchronizing the receiver and transmitter based on the clock correction parameter; and repeating the estimating, computing and synchronizing steps for a next window.

However, Kleider et al. discloses in Fig(s). 7A-7C, a method for synchronization wherein he discloses obtaining a window length from an experimental knowledge base (Kleider et al. discloses choosing an appropriate window resolution for y(n) (col. 10, lines 30-32); forming a window using the window length (Fig(s). 7A-7C); estimating the frequency and phase drifts between the transmitter and the receiver clocks using an input pilot signal and the window (col. 7, lines 27-30; 65-66; Kleider et al. discloses y(n) comprising a pilot sequence; col. 10, lines 30-33; Kleider et al. discloses timing (phase) and frequency offsets; also lines 43-53); computing the clock correction parameter based on the phase and frequency drifts; synchronizing the receiver

and transmitter clocks based on the clock correction parameter (Fig. 6, col. 6, line 60-col. 7, line 8; Kleider et al. discloses clock recovery (synchronization of transmitter and receiver clocks) based on sampling instant offset estimates (phase drift) and frequency offsets); and repeating the estimating, computing, and synchronizing steps for a next window (Fig. 7A-7C discloses example window lengths used for estimation of the offsets (pg. 10, lines 20-36). It would simply be inherent that the process would be repeated for each window.

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Kleider et al. as a method of synchronization and correcting timing alignment for multicarrier signals (col. 1, lines 34-37).

(4) With regard to claims 34, claim 34 disclose the method of claim 4 implemented by computer-executable instructions stored on a computer readable medium. As noted above, the combination of Hadad and Kleider et al. disclose all limitations of claim 4. Though neither Hadad nor Kleider et al. disclose the method implemented by computer-executable instructions, such a method implemented by computer-executable instructions instead of the hardware as disclosed by the references would be simply a design choice, since it is well-known in the art to implement hardware functions by computer-executable instructions. One of ordinary skill in the art would have been motivated to implement the design by computer-executable instructions for reliability, cost saving and ease/simplicity of parameter changes.

(5) With regard to claim 37, claim 37 discloses the method of claim 8 implemented by computer-executable instructions stored on a computer readable medium. As noted, the combination of Hadad, Kleider et al. and Sawahashi et al. disclose all limitations of claim 4. Though neither of the references explictly discloses the method implemented by computer-

executable instructions, such a method implemented by computer-executable instructions instead of the hardware as disclosed by the references would be simply a design choice, since it is well-known in the art to implement hardware functions by computer-executable instructions. One of ordinary skill in the art would have been motivated to implement the design by computer-executable instructions for reliability, cost saving and ease/simplicity of parameter changes.

5. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hadad (US Patent 6,985,432 B1) in view of Kleider et al. (US Patent 6,487,252 B1) as applied to claim 1 above, and further in view of Sawahashi et al. (US Patent 5,694,388).

Claim 8 inherits all limitations of claim 1 above. As noted above, the combination of Hadad and Kleider et al. disclose all limitations of claim 1. They do not explictly teach wherein estimating the phase drift comprises: estimating a reference phase; estimating the phase of the input pilot signal; and obtaining the phase drift by using the estimate of the phase of the input pilot signal and the estimated reference phase.

However, Sawahashi et al. teaches wherein estimating a phase drift (error) comprises: estimating a reference phase; estimating the phase of the input pilot signal; and obtaining the phase drift (error) by using the estimate of the phase of the input pilot signal and the estimated reference phase (col. 24, line 61-col. 25, line 3).

It would have been obvious to one skilled in the art at the time of the invention to incorporate the teachings of Sawahashi et al. to obtain an accurate measure of phase drift/error in the signal.

(2) With regard to claim 9, Hadad also discloses in Fig. 3, wherein synchronizing the receiver clock with the transmitter clock further comprises: synchronizing the receiver clock with the transmitter clock by correcting for the phase drift (ASC) substantially after correcting for the frequency drift (AFC). Hadad discloses the AFC being applied well before the ASC since it is well known in the art that frequency drift results in phase drift.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hadad (US Patent 6,985,432 B1) in view of Kleider et al. (US Patent 6,487,252 B1) as applied to claim 10 above, and further in view of Sawahashi et al. (US Patent 5,694,388).

Claim 13 inherits all limitations of claim 10 above. As noted above, the combination of Hadad and Kleider et al. disclose all limitations of claim 10. They do not explictly teach wherein estimating the phase drift comprises: obtaining an estimate of the input pilot signal; and obtaining the phase drift by using the estimate of the phase of the input pilot signal and a predetermined reference phase.

However, Sawahashi et al. teaches wherein estimating a phase drift (error) comprises: obtaining an estimate of the phase of the input pilot signal; and obtaining a phase drift (error) by using the estimate of the phase of the input pilot signal and a predetermined reference phase (col. 24, line 61-col. 25, line 3).

It would have been obvious to one skilled in the art at the time of the invention to incorporate the teachings of Sawahashi et al. to obtain an accurate measure of phase drift/error in the signal.

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hadad (US Patent 6,985,432 B1) in view of Heidari et al. (US Patent 7,035,326 B1).

Claim 24 inherits all limitations of claim 23. As noted, Hadad discloses all limitations of claim 23. Hadad does not explictly disclose wherein the local receiver and the remote transmitter comprise a Digital-to-Analog Converter (DAC) and an Analog-to- Digital Converter (ADC), and wherein the clock correction module is configured to synchronize the local receiver ADC and DAC clocks with the remote transmitter ADC and DAC clocks using the clock correction parameter.

However, Heidari et al. discloses in Fig. 2A, wherein the local receiver and the remote transmitter comprise a Digital-to-Analog Converter (DAC, 224A) and an Analog-to- Digital Converter (ADC, 278A), and wherein a synchronization module (200) is configured to synchronize the local receiver ADC and DAC clocks with the remote transmitter ADC and DAC clocks (col. 6, lines 21-24).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Heidari et al. to insure synchronization between the transmitting and receiving devices for accurate data flow.

8. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hadad (US Patent 6,985,432 B1) in view of Heidari et al. (US Patent 7,035,326 B1).

(1) With regard to claim 38, Hadad discloses in Fig. 3, a computer system for synchronizing clock signals in a communication system used in a multi-carrier system, comprising: a data sampler (Fig. 3, Pilot Ext, 27) to sample an input pilot signal of a

predetermined carrier frequency and phase (col. 8, lines 47-50); a frequency drift estimator (AFC; col. 6, lines 35-37), coupled to the data sampler, to receive the data signal along with the input pilot signal, and to estimate a frequency drift between the receiver and transmitter clocks using the input pilot signal; a phase drift estimator (ASC; col. 6, lines 15-24), coupled to the data sampler and the frequency drift estimator, to receive the data signal along with the input pilot signal, and to estimate a phase drift between the receiver and transmitter clocks using the input pilot signal; an analyzer, coupled to the frequency drift estimator (AFC, col. 9, lines 61-65; Hadad discloses the AFC detects a frequency error from the pilots and issues a correction signal (clock correction parameter). Thus the AFC also acts as an analyzer since a frequency error is detected and based upon this frequency error, a corrected timing signal is created) and the phase drift estimator (Hadad discloses the ASC detects the slope of the phase of the pilots and computes a synchronization error, and supplies a corrected timing signal (clock correction parameter). Thus the ASC also functions as an analyzer, since it detects the slopes of the phase of the pilots and based upon this phase computes an error and supplies a corrected timing signal) to receive the estimated phase and frequency drifts, and to compute a clock correction parameter (both ASC and AFC compute a corrected timing signal) based on the received estimated phase and frequency drifts; and a synchronizing block (NCO, 26, VCO, 23), coupled to the analyzer, to receive the clock correction parameter, and to adjust the receiver clock to synchronize the receiver clock with the transmitter clock based the clock correction parameter (col. 9, lines 22-30, 56-65).

Hadad does not explictly disclose a bus, a processor coupled to the bus; or a memory coupled to the processor. However, Heidari et al. discloses in Fig. 2A a synchronization module

(200) comprising a bus (shown by dotted lines), a processor (228A) coupled to the bus; a memory (230A) coupled to the processor (228A).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Heidari et al. as a method of implementing a computer based synchronization module.

Allowable Subject Matter

9. Claims 15, 18-22 are allowed.

10. Claim 5-7, 12, 14, 25-29, 31-33, 36, 39-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
January 4, 2008

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER